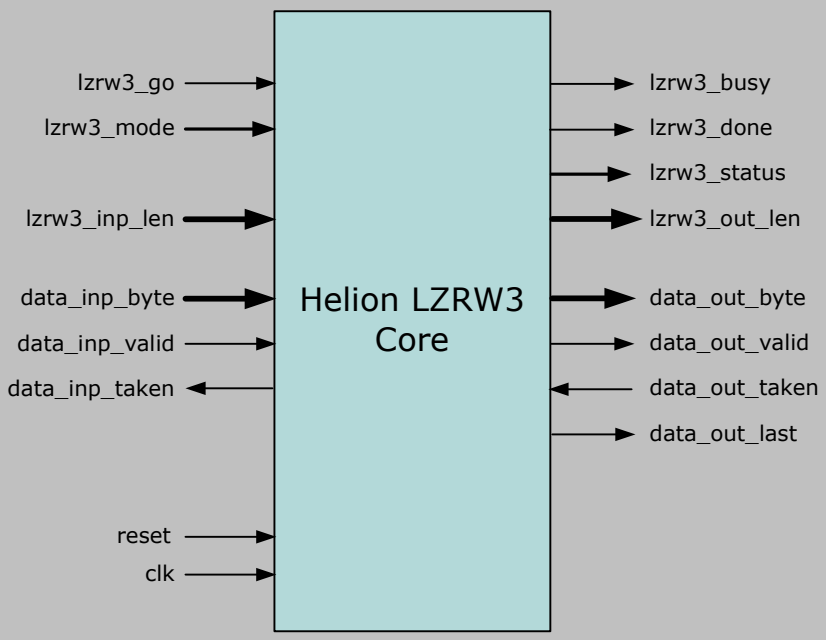
Helion Technology

FULL DATASHEET – LZRW3 Data Compression Core for Xilinx FPGA



Features

- Implements the LZRW3 lossless data compression algorithm
- Available as Compress only, Expand only, or Compressor/Expander core
- Supports data block sizes from 2K to 32K bytes with data growth protection
- Completely self-contained; does not require off-chip memory
- High performance; capable of data throughputs in excess of 1 Gbps
- Highly optimised for use in Xilinx FPGA technologies
- Ideal for improving system performance in data comms and storage applications

Deliverables

- Target specific netlist or fully synthesisable RTL VHDL/Verilog
- VHDL/Verilog simulation model and testbench
- Comprehensive User documentation

Overview

The Lempel-Ziv (LZ) compression methods are among the most popular algorithms for lossless data compression. LZ methods use a table based compression model where table entries are substituted for repeated strings of data.

LZRW3 is a well known LZ-type algorithm developed by Ross Williams in the 1990s which offers a useful combination of high throughput and good compression performance. It also has the advantage of being very efficient to build in hardware, unlike the majority of compression algorithms which tend to favour software implementations.

The Helion LZRW3 core implements the LZRW3 data compression algorithm in Xilinx FPGA without the need for external memory storage. It is capable of handling data throughputs in excess of 1 Gigabit/sec, and is ideal for use for improving system performance and efficiency in data communications, networking and data storage applications.

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General Description

The Helion LZRW3 core operates on one input block at a time (see later section for more information on block sizing). An LZRW3 operation is started whenever the "go" input to the core is asserted and the core is not busy. The data input length and mode inputs need to be valid during the go cycle, after which the processing starts; the core busy flag is asserted whilst compression or decompression is in progress.

Whilst the core is busy, data can be passed into the core for processing. The data input and output interfaces are byte-wide, and use associated ready/taken data flow control signals to transfer data to/from the core. Input data is pushed into the core by the user application, and output data is pushed out from the core to the user application.

Once a whole data block has been processed, a single cycle pulse is output on "done" to indicate when the core is finished as well as to indicate the output length in bytes and status outputs are valid. The status output shows whether the compression attempt was successful or not. Further block processing can then be started.

The Helion LZRW3 core processes data at a *peak rate* of 1 byte per clock on the fastest (uncompressed) interface; obviously the slower interface (compressed) will be at a lower rate than this. The actual rate depends on exactly what is happening in the internal pipeline at any one time, which by the very nature of data compression/expansion is data dependent. As a generalisation however, the data rate is typically 70-90% of this maximum, and the performance figures given in the tables below assume a typical throughput of 0.8 bytes per clock for both compression and expansion. Since this is a complex area, please feel free to contact Helion for full background on both compression and throughput performance of these cores.

Logic Utilisation and Performance

The tables below show typical logic area and performance figures for each version of the core covering two of the most popular Xilinx device families. All figures shown are for versions of the core supporting a maximum block size of 2K bytes.

	LZRW3 Comp		**LZRW3 Exp**		**LZRW3 Comp/Exp**	
technology	Spartan3E -5	Virtex5 -3	Spartan3E -5	Virtex5 -3	Spartan3E -5	Virtex5 -3
logic resource	787 slices 4 RAMB16	190 slices 4 RAMB18	794 slices 4 RAMB16	166 slices 4 RAMB18	885 slices 4 RAMB16	213 slices 4 RAMB18
max clock	103 MHz	215 MHz	110 MHz	226 MHz	106 MHz	205 MHz
typ throughput	659 Mbps	1376 Mbps	704 Mbps	1446 Mbps	678 Mbps	1312 Mbps

Please note: the cores are available with support for larger block sizes (see later), and also for use with almost all other Xilinx FPGA families (both old and new). Area and performance figures are available from Helion on request for all these variants and for all device types and speed grades.

LZRW3 – Choice of Blocksize

The generalised LZRW3 algorithm works on data streams with an unbounded history size. However, for a fast hardware implementation it is desirable to use local storage such as Xilinx BlockRAM for the history, and therefore the history size must be bounded to a sensible value by introducing a maximum block size.

The Helion LZRW3 core supports maximum block sizes from 2K bytes upwards in power-of-two increments to 32K bytes. The next section lists the actual amount of RAM required for each blocksize; as you can see the number of BlockRAMs used by the core increases significantly with the supported data block size whilst the logic area increases only slightly. It should be noted that 4K bytes is particularly efficient using Xilinx BlockRAM.

For packet based systems with defined maximum packet sizes, the whole packet can be handled in a single LZRW3 operation. For stream based systems with very long data streams, these must be formed into multiple blocks which are compressed using independent LZRW3 operations. For many applications suitably sized data blocks may already exist within the system, so the core can be sized accordingly. When defining the block size, a trade-off exists between the amount of local history storage required and the resulting compression efficiency, since longer blocks in general tend to compress better. Helion have modified the algorithm slightly (whilst maintaining full compatibility with the LZRW3 standard) to achieve better compression results for very short packets.

Please feel free to contact Helion to discuss the best choice of blocksize for your particular application.

Internal RAM Requirements

The utilisation of embedded RAM depends only on the chosen blocksize; the RAM requirements are the same for each variant of the core (compresss-only, expand-only, compress/expand). The table below lists the required numbers of BlockRAMs for each supported LZRW3 blocksize in current Xilinx technologies.

Note also that the logic area also slightly increases for larger blocksizes, and the maximum supported clock rate may be affected. Please contact Helion for full details for the specific variant you are most interested in.

blocksize (bytes)	2K	4K	8K	16K	32K
number of RAMB16s in Spartan3 & Virtex4	4	5	8	12	20
number of RAMB18s in Virtex5	4	5	8	12	20

About Helion

Founded in 1992, Helion is a well established British company based in Cambridge, England, offering a range of product-proven Data Security IP cores backed up by highly experienced and professional design service capabilities.

Although we specialise in providing the highest performance data encryption and authentication IP, our interest does not stop there. Unlike broadline IP vendors who try to supply a very diverse range of solutions, being specialists we can offer much more than just the IP core.

For instance, we are pleased to be able to supply up-front expert advice on any security applications which might take advantage of our technology. Many of our customers are adding data security into their existing systems for the first time, and are looking for a little assistance with how best to achieve this. We are pleased to help with suitable advice and support where necessary, and pride ourselves in our highly personal approach.

In addition, our Design Services team have an impressive track record in the development of real security products for our customers; we are proud to have been involved in the design of numerous highly acclaimed security products. This knowledge and experience is fed back into our IP cores, to ensure that they are easy to integrate into real systems, and perform appropriately for real engineering applications.

Helion is also a member of the Xilinx AllianceCORE IP program, and a certified Xilinx Alliance Partner. We therefore take our Xilinx implementations very seriously indeed. Our cores have been designed from the ground up to be highly optimal in Xilinx FPGA; they are not simply based on a generic ASIC design like much of the competition.

Most Helion IP cores make use of Xilinx-specific architectural features; in fact in many cases we build-up custom internal logic structures by hand, in order to achieve the very highest performance and most efficient logic resource utilisation. The benefits of this dedicated approach can be clearly demonstrated by direct comparison between Helion data security IP cores and the equivalents from other vendors.

More Information

For more detailed information on this or any of our other products and services, please contact Helion and we will be pleased to discuss how we can assist with your individual requirements.

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